Collaboration through Industry Standards for Manufacturing Success

Dave Dowding, Andrew Hildebrant, Domenico Chindamo, Jeff Rearick
Agilent Technologies, Inc.
815 14th Street S. W. MS DL416
Loveland, Colorado 80537
dave_dowding@agilent.com

Abstract

System-on-Chip designs are challenging Design-to-Manufacturing integrated tool suites that were thought to be comprehensive. Emerging methodologies and continued complexity of new designs keep pushing Electronic Design Automation tools and Automatic Test Equipment platforms beyond past limitations. Greater integration of new tools and platforms are based in immerging industry standards. How these standards are beginning to be used to integrate tools and platforms into viable solutions is the focus of this paper.

The System on Chip (SoC) Level Integrated Circuit (IC) New Product Flow in Constant Change

Design and test development automation have provided the semiconductor industry with significant capabilities to produce increasingly complex devices in a timely fashion. Developing and integrating these tools into a new product development flow is, in itself, a significant accomplishment.

Tool development and integration has long provided a competitive Time-to-Market (TTM) advantage for semiconductor companies. This advantage is achieved by the smooth transfer of data between various points of the design, test development and manufacturing processes.

Automation tools exact a recurring cost. The steady march of Moore's Law increases gate count and introduces new technology challenges. In order for a semiconductor company to remain competitive, its tools must track technology advances. The term "tool" here refers to Electronic Design Automation (EDA) tools such as Design-For-Test (DFT) Automatic Test Pattern Generation (ATPG) tools, design integration tools, and Fault Localization (FL) and Failure Analysis (FA) tools [1]. This term also applies to Automatic Test Equipment (ATE), and includes the tester operating system and utilities, as well as the test development tools used to prepare EDA output for the tester.

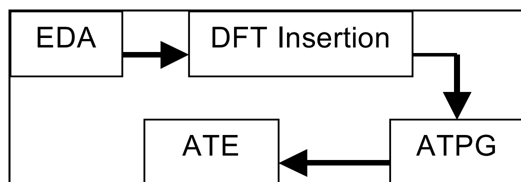

Figure 1: Typical Semiconductor Device Product Development Flow

As shown in Figure 1, the integration of tools is focused on providing data alignment between one step and the next. One third-party test development package creates several intermediate data formats to deal with different types of input design data, and other formats to deal with their ATE bridge tools. The problem with progressing with technology advancements is that you must continuously change your tools and methodologies, and the data and formats must change to follow those advancements.

Companies that elect to manage in-house tool development and integration must staff tools groups and provide the connection between the internal and commercial tools. In the past, larger semiconductor manufacturers often established their own data formats to help unify the product development flow.

Companies that acquire this integration from outside purchase these services from the tool vendors or others. They often incur development delays and significant costs and may not achieve the level of integration and specialization they need. Despite these difficulties, semiconductor manufacturers address their new product development needs by one or the other approach, or the combination of both.

In recent years, the rising complexity of semiconductor designs has come into direct conflict with shorter TTM goals, and resulted in lower margins [2]. In order to meet new product market windows, semiconductor companies must now integrate commercial toolsets that track fast paced technology changes. In-house tools can be prohibitively expensive or too slow to adapt these technology trends. Commercial vendors can no longer afford the cost of targeting custom interfaces on a customer-by-customer basis. The proprietary in-house "standards" that once afforded semiconductor companies with tight integration have, in many cases, become the barrier to the adoption of rapid technology advancements via commercial tools.

Industry Standards Reintegrate Design, Test and Manufacturing

Semiconductor, EDA and ATE companies have responded to technology's challenges and changes by forming industry standards efforts to provide common interchange "language" standards that address the data flow from design through manufacturing for both manufacturers and tool vendors. The objectives in adopting these standards are:

- Reduced integration efforts and costs
- Help overcome the TTM barrier caused by "in-house" proprietary formats
- Support immerging DFT technologies, such as BIST (Built-In Self Test), which will, in turn, improve manufacturability.

When vendors and manufacturers join together, they can cause a "re-integration" of new product development flows with off-the-shelf tools and equipment. These joint activities have real costs, however, early adopters can enjoy

reintegration cost advantages earlier, and overall the industry is enabled to advance beyond the current challenges.

Design Automation Lead the Trend

In the typical semiconductor product development flow, a design team selects an EDA tool suite that addresses the design and test methodology they wish to use. In the past, the design teams may have been able to choose to have those tools built in-house or to purchase and integrate commercial tools, all depending on technology challenges, TTM pressures and personnel constraints. Due to industry economics, the cost of developing and maintaining in-house solutions may become prohibitive. But that aside, the tools must operate efficiently, and they must leverage, whenever possible, on common data formats.

As design automation tools were developed, industry standard formats were introduced. For example, Verilog and VHDL standards, when first introduced, shared the same simulation dump file format. Later, design tools that supported one or the other standard had offerings that were interoperable with both. The development of these design standards helped ensure that whatever design tool suite was selected, the data from it could be connected to downstream tools.

Automation in DFT Insertion and Test Generation Data Format Gap

As design automation progressed, larger designs could be accomplished more quickly. DFT test techniques were developed improved test coverage and testability on the larger designs. As design complexity grew, so grew the semiconductor manufacturer's reliance on DFT methodologies. EDA tools then provided automated scan insertion and scan test generation, thus adding significant capabilities and TTM advantages.

The commercial scan ATPG tools that followed the scan insertion tools had to target their test data in various formats, since there was no standard in place. A pseudo standard of "WGL" was commonly offered, but larger semiconductor vendors had their own in-house data formats as well. This diversity of output formats cost both vendors and users tool integration and translation efforts. Even though the design team started with industry-standard interfaces in their EDA tools, there was a data interchange gap at the output of the ATPGs.

The IEEE 1450-1999 Standard and EDA

With the IEEE's "1450-1999 Standard Test Interface Language Std." or "STIL" (pronounced style), the data interchange gap was addressed. This standard addresses the digital device test constructs for functional and structural test data. The DFT EDA tools can output to STIL and utilize its ever-expanding extensions to take advantage of new test methodologies encompassed therein.[3] Now, EDA vendors can focus on the solutions to address new technology challenges, and implement them in specific design methodology tools.

An example of new methodologies for SoC manufacture is the immergence of the P1450.6 Core Test Language (CTL) extension to STIL[4]. Using this extension, core providers, package with the IP cores test methodology and its test data. The supplied test methodology is validated to the boundary of the IP core. EDA integration tools can use CTL to integrate the various cores to produce an integrated device with test methodologies that are correct by construction to the boundary of the SoC. This approach reduces the risk and development time to produce a complex SoC device.

Advantages of Using STIL on ATE

For even a completely custom device, the Design team can now transfer the ATPG output to the Test team for deployment onto ATE. Before the STIL standard, this was accomplished in one of two ways. Larger semiconductor manufacturers built internal translation tools that bridged in-house design tools to the specific tester formats they had on their test floor. Other companies purchased off-the-shelf translation tools and integrated them into their design flow. In either case, there is usually more than one ATE platform to be targeted, each with its own data format.

Today, the cost of transporting test data via the STIL format is reduced dramatically. Some ATE platforms operate with the STIL data directly, without external translation. Other ATE platforms provide front-end tools to consume the design generated STIL format and convert it to an efficient, directly loadable format that has hardware accelerator advantages. By using tools based on the standard interface of STIL, the Design and Test teams now enjoy a lower cost of tools integration, and the simplified ATPG-to-ATE translations lower infrastructure costs to provide a faster TTM.

Standards Alliances Advance the Industry

With the rise of EDA and ATE alliances around STIL and other standards, many common ATPG and ATE packages have been pre-validated by the vendors, further reducing the integration challenges faced by their customers. These alliances validate the interoperability of STIL from various EDA tools to and between various ATE platforms.

These alliances provide a common ground for semiconductor manufacturers, EDA tool vendors and ATE providers to integrate and validate new tools and flows. The vendors can leverage greater use from their efforts, and semiconductor manufacturers reduce their integration costs.

Industry Examples of Standards Improvements

The implementation and utilization of standards to address industry issues will be discussed next. Three examples will show different uses of the STIL standard and its extensions to provide solutions, reduce costs and yield better TTM.

Example #1: ATPG Targeting the Actual Tester Resource Configuration

Our first example considers the concept of ATPG generated tests that are "correct by construction" via the proposed IEEE P1450.3 Tester Targeting STIL Extension. One of the purposes of this extension to STIL is to encapsulate a description of the tester resources' capabilities, limits and restrictions in standard constructs[3]. It is intended, that through a P1450.3 description, semiconductor companies can represent their testers' configurations to commercial design tools.

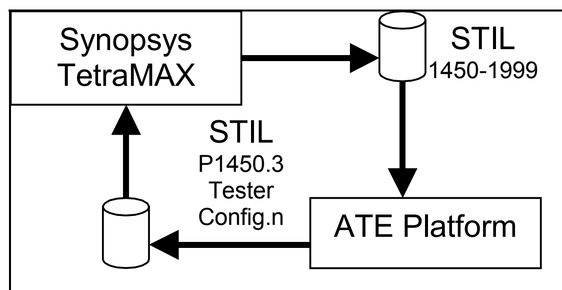

Figure 2: EDA tools directed by P1450.3 Tester Targeting extension configurations obtained from ATE platform

The validation offered by STIL P1450.3 serves two main purposes. First, design tools are able to use the tester's configuration to guild the EDA tools, so that the test data they produce will load and run on a specific model of ATE. This is the concept of "correct by construction". All to often, test development tools had insufficient ATE configuration descriptions to accurately guide their output. Using the P1450.3 ATE configurations, the Design and Test teams will know that the deployment of test data will be loadable on the target ATE. EDA and ATE companies that provide P1450.3 tester configurations help the semiconductor companies ensure that test data their EDA tools generate will avoid first silicon false starts and recurring test development costs.

Secondly, having early knowledge of ATE configurations allow semiconductor companies to treat ATE as a "black box" for many types of tests. The selection of test services contractor is often done far in advance of the fabrication of any silicon. Since the test services contractors can now express their ATE configurations in the P1450.3 constructs, this allows the semiconductor companies to make a pre-validated decision regarding their production test deployment and costs. Many basic and advanced ATE resource capabilities are covered in STIL P1450.3, thus enabling the semiconductor company to focus its effort on the most difficult or exotic test challenges.

Example #2: ATPG to ATE and Back

Our second example of industry standards leveraging considers the scenario where Synopsys' SoCBIST methodology is implemented on a high-volume consumer device. The device is deployed for production test on a high volume SoC-series ATE platform.

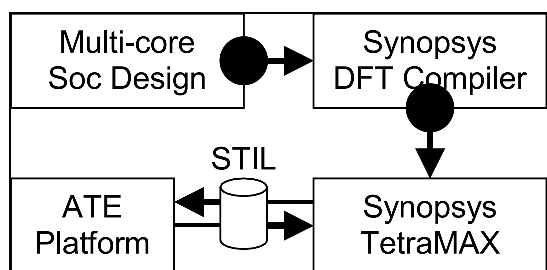

Figure 3: Synopsys SoCBIST Flow to the ATE Platform

The customer's first challenge is the integration of several custom digital IP cores into the overall SoC design. The design team elects to implement a core with a P1500 embedded core wrapper. The digital cores are all tested via DC scan, supplied to the design team by the core provider. The test data is represented in the IEEE P1450.6 Core Test Language.

During floor planning, the design team decides that the largest digital core, a 32-bit microprocessor, cannot be tested from the boundary of the device due to an unacceptable tradeoff between restricting external access pins and a longer test time. The team elects to use Synopsys SoCBIST, a digital logic BIST technology.

Synopsys integration tools support the industry standards of IEEE P1500 and IEEE P1450.6. As a result, the application of SoCBIST to the digital core requires a minimal amount of custom work and proceeds quickly.

After the Design team has run the Synopsys tools to integrate the cores (which had CTL protocols to the boundary of the individual cores), they then run Synopsys TetraMAX ATPG to generate all the test CTL protocols to the boundary of the SoC device. Having represented the core test methodology and hierarchy in CTL, the TetraMAX ATPG now provides the test patterns, timing and test data in IEEE 1450-1999 and P1450.1 STIL to the boundary of the SoC[5].

The Test team is able to immediately start working with the CTL and STIL data in an ATE supplied, off-the-shelf CTL browser product. This CTL package supports the STIL series of IEEE standards, allowing the test team to easily generate a test program for their SoC series production testers. Again, little custom work is required, because both the EDA and ATE vendor products are connecting via a documented industry-standard interface.

Test Results Back to EDA Failure Analysis Tools

The Test team uses an additional ATE vendor supplied application that operates the SoCBIST engine on the tester. The customer intends that every 1000th failing device should be sampled in the SoCBIST diagnostic mode. This mode of operation passes data out to the ATE to be captured. The captured data will be sent back to Synopsys TetraMAX for fault analysis. Software fault isolation can be much faster than physical failure analysis, and can be used to guide the FA engineers directly to the x-y coordinates of specific failures. In turn, the timely examination of physical defects and marginalities allows the manufacturing process team to accelerate yield improvement.

The captured data is to be sent back to Synopsys TetraMAX in the IEEE P1450.1 failure data format. Using this portion of the proposed standard at the ATE boundary, allows the consulting team to focus their efforts on adapting the special capabilities of the ATE platforms to work with the Synopsys SoCBIST diagnostics engine. As long as the standard is used at the tester boundary, the ATE vendor can expand their application to support other LBIST engines. In a similar manner, Synopsys is only burdened with the support of a single, industry-standard interface to all ATE vendors.

In this scenario, the standard allows both the EDA and ATE vendors to focus on enhancing the unique capabilities of their products. An EDA-ATE technology alliance based on the STIL standard ensures the removal of interoperability

barriers, granting their customers a very low integration cost, accelerated TTM and easy access to advanced yield improvement technologies.

Example #3: ATE and Design Validation Test Data Interoperability

Our third example considers the application of industry standards to transfer test data between a desktop DFT Design Validation (DV) unit and a high-volume production ATE system [6].

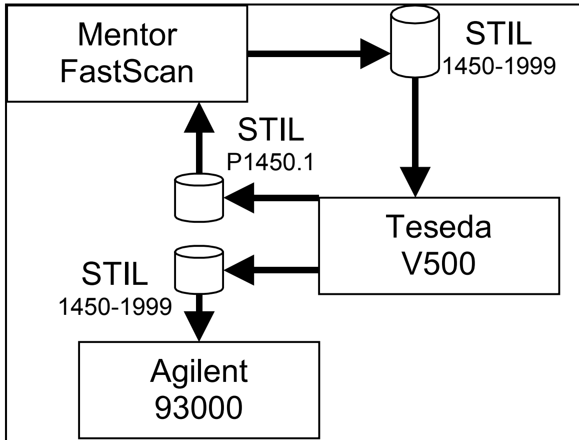

Figure 4: DFT ATPG tests debug on a desktop Design Validation system leading to production deployment on a production ATE platform

In order to accelerate DFT validation, a customer purchases multiple V500 desktop units from Teseda. These desktop units will be directly available for designers to perform first silicon validation, and eliminate the need for them to share time slots with the Test-engineering group that owns the high volume ATE systems. This approach enables the designers to work in parallel when validating digital cores or debugging individual DC and AC scan tests. At the same time, the test-engineering team will complete debug of the SoC's high-speed interface and multiple mixed-signal/analog cores on the production ATE.

Once all the tests are validated or debugged, the designers and test engineers must integrate the test data into a single production test flow. Traditionally it has been a major challenge to port data between different DV and ATE systems. The custom tools to provide this port require both time and engineering expense to develop. However, both systems have STIL in common. The Teseda system is a "STIL native" validation unit, indicating that it can both read in and write out STIL test data, and the Agilent 93000 toolset can port the STIL data into its native format.

Since both ATE platforms can communicate via a common STIL specification, there is no translation or integration cost for the customer. To further guarantee interoperability, Teseda and Agilent have verified that the STIL output of the V500 DFT validation unit will load and operate correctly on an Agilent 93000 SoC tester.

This vendor guarantee helps to reduce the TTM risk for the customer. The design team is now free to do basic DFT validation in parallel with the test team's characterization and debug activities on the target production platform. The industry-standard interface of STIL provides a fast, supported method to transfer the debugged DFT test data from the desktop validation unit to the final production ATE.

In Conclusion:

The immerging interfaces provided by industry standards and their extensions provide the following benefits:

1. Improve TTM by reducing or eliminating integration overhead
2. Lower the integration costs by ensuring interoperability
3. Provide uniform tool and platform advanced capabilities with lower barrier-to-entry for customer usage
4. Catalyze industry alliances by creating standard interfaces that achieve critical mass, thus drawing a steady focus of resources
5. Allow vendors to focus on offering innovative technologies to address specific design or test challenges, instead of forcing them to invest in scattered proprietary software or one-size-fits-all hardware. ATE vendors can focus on better utilization of tester resources and new capabilities. EDA vendors will focus on easier integration of new technologies, thus lowering the customer's barrier to entry.

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